

# ABSTRACT OF THE DISCLOSURE

There is provided a semiconductor storage device in which only a defective element is replaced by a row redundant element to compensate for a defect if at least one of a plurality of elements is defective in a case where the plurality of elements in a memory cell array are simultaneously activated. The semiconductor storage device includes an array control circuit which is configured to interrupt the operation of the defective element by preventing a word line state signal from being received based on a signal to determine whether a row redundancy replacement process is performed or not. The word line state signal is input to the plurality of memory blocks in the cell array unit via a single signal line.